ISSN 2229-5518

Selective Harmonic Elimination In UPS – A Survey

E.Anandha Banu, Dr.D. Shalini Punithavathani

Abstract— Uninterruptable power supplies (UPS) are widely used to supply critical loads and provide reliable and high quality energy to the load. Inverter is the main component of UPS. In this majority of power utilities are non linear loads, so there is a possibility of generation of harmonics. This paper presents a survey of different topologies, control strategies and modulation techniques used by UPS. The multilevel concept is used to decrease the harmonic distortion in the output waveform without decreasing the inverter power output. This paper presents the most important topologies like diode-clamped inverter (neutral- point clamped), capacitor-clamped (flying capacitor), and cascaded multilevel with separate dc sources. This paper also presents the most relevant control and modulation method that is selective harmonic elimination. Here, in the existing literature, all the methods, which are already available for harmonic elimination in UPSs, are discussed and the best suited method is found out that is with low total harmonic distortion and with less computational time and the future work how it can be extended.

Index Terms— Harmonics, Modulation Techniques, Multilevel Inverter, Non Linear Loads, Selective Harmonic Elimination, Total Harmonic Distortion, UPS

1 INTRODUCTION

IN today's modern world, all industries pay great attention to different energy conservation programs and green initiatives. Hence, efficient electrical energy usage is becoming more of a concern, than in the past and electrical energy costs play an important role in the day-to-day business operations. In the recent times, since we are making use of a lot of Semiconductor devices, the technologies related to power electronics have drastically developed for different modern applications, such as uninterruptible power supply (UPS) systems, lighting and adjustable speed drivers (ASD). Non-sinusoidal current owing to non-linear loads causes a non-sinusoidal voltage. The usage of these equipments draws non-sinusoidal current and hence results in the harmonic distortion. Nowadays, the input stage of active electronic power converters is responsible for most of the harmonic distortions. The Power Quality (PQ) in power systems is significantly reduced by the Harmonic distortion due to non-linear power electronic equipments. In these days, PQ has become an important factor in differentiating between successful utilities in the power systems. In order to mitigate the undesirable effects of harmonics on PQ, various techniques such as the application of harmonic filters, modification of electric circuit configurations, the choice of transformer connections and the use of higher-pulse converters, have been proposed. Active power filters were developed for harmonic compensation and power factor correction[1].Although UPS devices are economical, flexible and energy efficient, they may degrade power quality by creating harmonic currents and consuming excessive reactive power [2].Harmonics causes malfunctioning of electrical/electronic parts, overheating of neutral wires, transformer heating, and malfunctioning of power factor correction capacitors, power generation and transmission losses, disruption of protection, control and communication networks as well as customer loads.[3]

Harmonics is the main issue with inverters especially with those inverters used in the Uninterrupted Power Supplies (UPS). Though the sinusoidal and space vector types of PWM (SPWM & SVPWM) used in inverters help reduce harmonics they incur high switching losses. Therefore the selective harmonic elimination is nowadays coming up as an alternative for SPWM and SVPWM. In square wave inverters usually with single pulse scheme all the odd harmonics are present. However with SVPWM and SPWM techniques the harmonics are eliminated up to the switching frequency. In selective harmonics elimination only the lower order harmonics typically the 5th 7th 11th and the 13th order harmonics are selectively eliminated in the process of the inverter operation itself. In addition, after the lower order harmonics are eliminated the higher order harmonics can be easily eliminated using passive filters. Implementation of selective harmonic elimination involves the finding of the appropriate switching instants by solving a set of transcendental trigonometric equations. The number of equations and the variables in the equations increase with the number of harmonics to be eliminated.

- *E.Anandha Banu is a reaearch scholar in Manonmaniam Sundaranar University, Tirunelveli, India, PH-8880177095 E-mail: banu3k@yahoo.co.in.*
- *Dr. D. Shalini Punithavathani is the Principal, Government College of Engineering, Tirunelveli, India.*

2 UPS SYSTEM DESCRIPTION

Uninterruptable power supply (UPS) systems are employed to supply the critical loads with continuous and high quality energy in facilities such as hospitals, data centers, and communication systems etc [4]. A high-performance UPS system should have a clean output voltage with low total harmonic distortion (THD) for linear and nonlinear loads, high efficiency,

great reliability and fast transient response for sudden changes [5]. The main components of the system are the diode rectifier, pulse width modulation (PWM) inverter, input/output filter, dc-link capacitor, battery charger and battery, battery on/off switch, and load transformer. The topology can operate in two different modes, namely, normal/charging and backup modes. In the normal /charging mode, the battery on/off switch is opened. Therefore, the ac mains supplies the load power throughout the PWM inverter and charges the battery at constant current as well. In the backup mode, the ac mains is not available and the battery on/off switch is closed. Thus, the battery supplies the load power [6].

There are three categories of UPS topology: Off-line UPS, Line interactive UPS and Online UPS. In off-line UPS, under normal mode, the power is supplied to the load and the battery is charged from the utility line and while in case of power failure, the battery supplies power to the load. The line-interactive UPS consist of two different possible topologies. One topology contains an inductor in series between the utility input and the load and a bilateral inverter in parallel with the load, acting as a backup for the utility line and interacting with the utility line when the energy is reversible. Although the other topology comprises two converters: one is in series with the utility source and the other is in parallel with the load. In online UPS, the utility line supplies power to the load via the rectifier during the normal operation and whereas in case of disruption, the battery supplies power to the load by means of the inverter [7] .

3 Inverter Topologies

The most attractive features of multilevel inverters are as follows.

1. They can generate output voltages with extremely low distortion and lower dv/dt.
2. They draw input current with very low distortion.
3. They generate smaller common-mode (CM) voltage, thus reducing the stress in the motor bearings. In addition, using sophisticated modulation methods, CM voltages can be eliminated.
4. They can operate with a lower switching frequency.

The three different major multilevel converter structures have been reported in the literature: cascaded H-bridges converter with separate dc sources, diode clamped (neutral-clamped), and flying capacitors (capacitor clamped).[8].

3.1 Diode-Clamped Inverter

The most commonly used multilevel topology is the diode clamped inverter, in which the diode is used as the clamping device to clamp the dc bus voltage so as to achieve steps in the output voltage. Thus, the main concept of this inverter is to use diodes to limit the power devices voltage stress. The voltage over each capacitor and each switch is Vdc. An n level inverter needs (n-1) voltage sources, 2(n-1) switching devices and (n-1) (n-2) diodes. By increasing the number of voltage levels the quality of the output voltage is improved and the voltage waveform becomes closer to sinusoidal waveform. Figure.1 shows a three-level diode-clamped converter in which the dc bus consists of two capacitors, C1, C2. For dc bus voltage Vdc, the voltage across each capacitor is Vdc/2 and each device voltage stress will be limited to one capacitor voltage level Vdc/2 through clamping diodes. To explain how the staircase voltage is synthesized, the neutral point n is considered as the output phase voltage reference point. There are three switch combinations to synthesize three-level voltages across a and n.

1. Voltage level Van= Vdc/2, turn on the switches S1andS2.
2. Voltage level Van= 0, turn on the switches S2 and S1′.
3. Voltage level Van= - Vdc/2 turn on the switches S1,S2′.

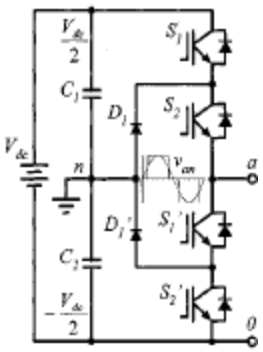

Fig.1. Diode-Clamped Multilevel Inverter Circuit with Three-Level.

3.2 Cascaded Multilevel Inverter

The concept of this inverter is based on connecting H-bridge inverters in series to get a sinusoidal voltage output. The output voltage is the sum of the voltage that is generated by each cell. The number of output voltage levels are 2n+1, where n is the number of cells. The switching angles can be chosen in such a way that the total harmonic distortion is minimized. One of the advantages of this type of multilevel inverter is that it needs less number of components comparative to the Diode clamped or the flying capacitor, so the price and the weight of the inverter is less than that of the two types.

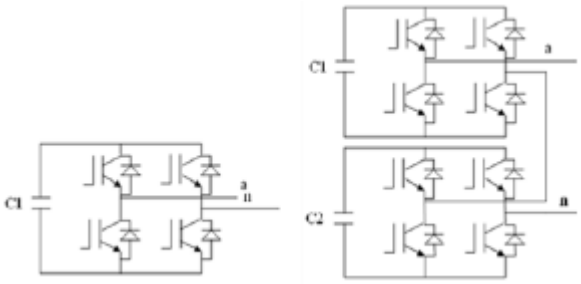

Fig.2. Single Phase Structures Of Cascaded Inverter (A) 3-Level, (B) 5-Level

Figure.2 shows the power circuit for one phase leg of a three-level and five-level cascaded inverter. In a 3-level cascaded inverter each single-phase full-bridge inverter generates three voltages at the output: +Vdc, 0, -Vdc (zero, positive dc voltage, and negative dc voltage). This is made possible by connecting the capacitors. The resulting output ac voltage swings from -Vdc to +Vdc with three levels, -2Vdc to+2Vdc.

ISSN 2229-5518

3.3 Capacitor Clamped Inverter

The structure of this inverter is similar to that of the diode clamped inverter except that instead of using clamping diodes, the inverter uses capacitors in their place. The flying capacitor involves series connection of capacitor clamped switching cells. This topology has a ladder structure of dc side capacitors, where the voltage on each capacitor differs from that of the next capacitor. The voltage increment between two adjacent capacitor legs gives the size of the voltage steps in the output waveform.fig shows single phase n-level configuration of capacitor clamped inverter. An n-level inverter will require a total of (n-1)×(n-2)/2 clamping capacitors per phase leg in addition to (n-1) main dc bus capacitors. The voltage levels and the arrangements of the flying capacitors in the FCMLI structure assures that the voltage stress across each main device is same and is equal to Vdc/(n-1), for an n-level inverter. The voltage synthesis in a five-level capacitor-clamped converter has more flexibility than a diode clamped converter.

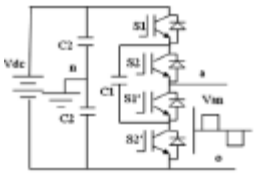

Fig.3. Capacitor-Clamped Multilevel Inverter Circuit Topologies with 3-Level Inverter

4 Classification Of Control Strategies

The main aim of the modulation strategy of multilevel inverters is to synthesize the output voltage as close as possible to the sinusoidal waveform. Many modulation techniques have been developed for harmonic reduction and switching loss minimization [9]. The modulation methods used in multilevel inverters can be classified according to switching frequency, as shown in Fig.4.

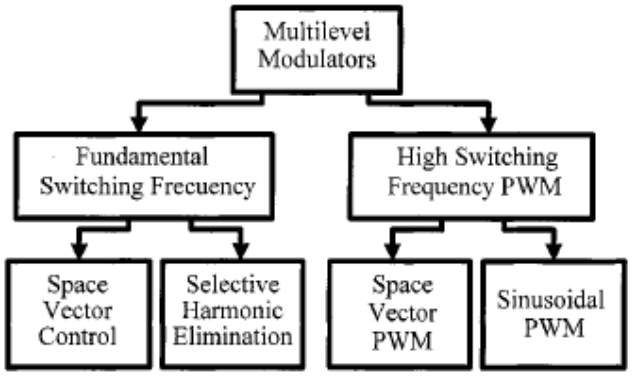

Fig. 4. Classification of multilevel modulation methods

Among these modulation methods, Selective Harmonic Elimination is being discussed here.

Selective Harmonic Elimination (SHE) is an off-line (precalculated) non carrier based PWM technique. In this method the basic square-wave output is "chopped" a number of times, which are obtained by proper off-line calculations [8]

Figure.4 shows a generalized quarter-wave symmetric stepped voltage waveform synthesized by a (2m+1) -level inverter, where m is the number of switching angles. By applying Fourier series analysis, the amplitude of any odd nth harmonic of the stepped waveform can be expressed as (4), whereas the amplitudes of all even harmonics are zero.

Where Vk is the Kth level of dc voltage, n is an odd harmonic order, m is the number of switching angles, and ak is the the switching angle. where a1 to am must satisfy

$a1 < a2 < a3 < \ldots\ldots < am-1 < am < \pi/2$

To minimize harmonic distortion and to achieve adjustable amplitude of the fundamental component, up to m-1 harmonic contents can be removed from the voltage waveform. In general, the most significant low-frequency harmonics are chosen for elimination by properly selecting angles among different level inverters, and high-frequency harmonic components can be readily removed by using additional filter circuits. To keep the number of eliminated harmonics at a constant level, all switching angles must be less than $\pi/2$.

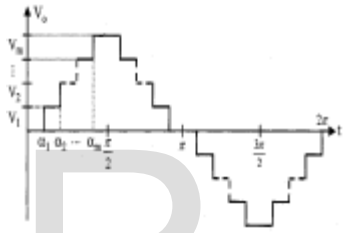

Fig.4. Generalized Stepped - Voltage Waveform

5 A Literature Survey Regarding With Selective Harmonic Elimination In UPS

Several literary works related to alleviation of harmonics are available in the literature. A few most recent research works in this topic are reviewed in this section.

Wells et al. [10] have proposed a modulation-based technique for generating pulse waveforms with selective harmonic elimination (SHE). Modulation index cannot be set exactly Is the drawback of this method. Ghennam, T. and Darwish, M. [11] have proposed a hybrid parallel active filter/offline UPS system for computer loads. Saied, B.M., Alias, Q.M. and AL-soufy, A.S [12] have investigated neural network and fuzzy logic-based SHE PWM technique. Here, the neural network (NN)-based fuzzy rules were affected by any interference problem.

Dahidah, M.S.A. and Agelidis, V.G. [13] have proposed a generalized formulation for SHE-PWM control, suitable for high voltage high-power cascaded multilevel voltage source converter (VSC).

Du et al. [14] have presented a reduced switching-frequency active-harmonic-elimination method. Jagdish Kumar, Biswarup Das, and Pramod Agarwal [15] have proposed Newton-Raphson method that produces all possible solution sets when they exist. The advantages are it can produce all possible solution sets for any numbers of multilevel inverter without much computational burden, speed,of convergence is fast etc.

Faiz, J. and Shahgholian, G. [16] and Faiz, J. and Shahgholian, G. [17] have proposed a control system and multiple filters for three phase PWM inverter connected to nonlinear load. Here, when the inverter level varies, the filter order gets changed is the drawback of multiple filters. A neural and neuro-fuzzy controller for enhancing the transient response and flexibility of the inverters of UPS to a variety of loads has been presented by Bhoopal, N. and Madhav, G.V. [18]. As well, Du et al. [19] have presented a cascaded H-bridge multilevel inverter that has been implemented using only a single dc power source and capacitors.

Salam, Z. [20] has proposed a HEPWM scheme for voltage source inverters (VSI) based on the curve fittings of certain polynomial functions. For controlling the modulation index of VSC, Nayeripour et al. [21] and Al-Othman, A.K.and Al-Mekhaizim, H.A. [22] have proposed a fuzzy linear regression model for computing the optimal solution set of switching angles. However, the fuzzy regression model is only applicable for linear optimization problem.

Zainal Salam and N.Bahari [23] have proposed an approach to use Differential Evolution search method to determine the switching angles of SHE-PWM. It has been shown that the method can accurately compute the SHE-PWM switching angles without having to make "correct" guesses on the initial values of the switching angles. Reza Salehithe et al. [24] have applied SHEPWM switching approach to multilevel inverters in order to eliminate the low order harmonics in a broad variety of modulation indexes. However, the harmful harmonics such as the fifth order harmonic still remain in the output waveform

Azab, M. [25] has proposed PSO-based SHE technique for controlling PWM inverter. However, it is difficult for adapting undefined switching angles using the proposed PSO-based harmonic elimination technique. Merry Gaisa, J. and Rajaram, M.[26] have proposed a technique that has utilized the fuzzy logic and artificial neural network for the optimal selection of switching angles. In the neural network-based controller, the training dataset is necessary for analyzing the load variation of UPS. However, the training dataset generation is one of the complicated processes. Antony Albert, A.V., Rajasekaran, V. and Selvaperumal, S. [27] have proposed a technique, which eliminates the harmonics by generating negative harmonics with switching angles calculated for selective harmonic elimination method. However, the SHE method was in competent in producing optimal switching angle.

Pandi Perumal, M. and Nanjudapan, D. [28] have presented an optimal solution for eliminating pre-specified order of harmonics of a multilevel inverter.

Also, Venkatramanan, C.B., Jayakumar, K.S. and Yuvarani, B. [29] have proposed SHE-PWM control for cascaded voltage source multilevel inverter based on genetic algorithm (GA) optimization. There was no absolute assurance that the GA will find the global optimum solution. Mitali Shrivastava, Varsha Singh and Swapnajit Pattnaik [30]have proposed to solve selective harmonics elimination problem in PWM inverters using artificial neural network. Ayoub Kavousi et al.[31] have proposed the bee algorithm for SHE in multilvel inverter and found that results show accuracy and ability of bee algorithm for convergence objectives. Also, solutions have near probability to attain global minimum for 1, 2, 5, and 10 times runs and this probability is higher than the same runs for genetic algorithm (GA). Suman Debnath and Rup Narayan Ray [32] have proposed genetic algorithm and particle swarm optimization (PSO) are used for THD minimization in Cascaded H-Bridge Multilevel Inverter.it is observed that GA technique provides superior performance compared to PSO as far as the minimization of THD is concerned.

Merry Geisa and M. Rajaram [33] have proposed hybrid technique utilises an iterative technique and fuzzy logic for the optimal selection of switching angles. Comparison result has proved that the proposed method was capable of achieving better performance and reduced computational time. Prashanth L Gopal and F.T Josh [34] have proposed the performance of cascaded multilevel inverter based computation of switching angle using Genetic Algorithm as well as conventional Newton Raphson approach and a significant improvement in harmonic profile is achieved in the GA based approach. Rupali Mohanty, Sthitaprajna Rath and Surya Prasad Mishra [35] have proposed a comparative study of harmonic elimination in cascade multilevel inverter using particle swarm optimization (PSO) and genetic algorithm for 11 level cascaded H bridge and found that PSO has better THD.

Ali Ajami, Mohammad Reza Jannati Oskuee, and Ata Ollah Mokhberdoran, [36] have proposed an the imperialist competitive algorithm (ICA) to determine the optimum switching angles of a 9-level inverter and also to exert the SHE-PWM problem with larger number of switching angles, Simulation and experimental results are provided for a 9-level inverter to confirm the accuracy of suggested method. Also to develop the sufficiency of the SHE to all range of modulation index a DC-DC converter is used to control the input DC voltage of the inverter which improves the SHE effectiveness on eliminating the undesired harmonics. B.Srava and B.Seshur [37] have proposed a adaptive hybrid technique that is it uses the fuzzy and artificial neural network in selecting switching angle.

6 SUMMARY

The total harmonic distortion (THD) and computational time for different methods like particle swarm optimization (PSO), genetic algorithm (GA), Bee Algorithm (BA), artificial neural network (ANN), fuzzy logic (FL), ANN and FL, enhanced hybrid technique (fuzzy logic and iteration technique)(FL+Iter.) are noted from literature for selective harmonic elimination in 7 level inverter and are listed below in Table 1 and a comparison chart is plotted in fig 5.

TABLE 1
THD AND COMPUTATIONAL TIME OBTAINED BY DIFFERENT METHODS

	THD%	Comp. Time
PSO	3.7257	1.880862
GA	3.7764	0.0049
BA	8.99	1.035
ANN	4.2373	0.2021
FL	1.8468	0.0795
ANN+FL	2.0713	12.724
FL+Iter.	1.0157	0.039475

FL+Iter.	1.0157	0.039475

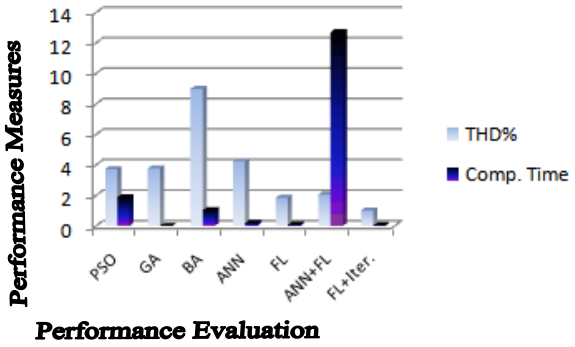

Fig.5. Comparison of different methodologies

In the above Table 1 , it is found that the enhanced hybrid technique is best suited with low THD and less computational time.

7 Conclusion

This paper has provided a brief summary of UPS, multilevel inverter circuit topologies and their control strategies especially selective harmonic elimination. A survey of several technical literature concerned with selective harmonic elimination in UPS with different methodology and according to literature it is found that the enhanced hybrid technique is best suited in reduction of total harmonic reduction with less computational time compared to that of other methodology .In future the work may be extended such that the applied methodology gives solution with less computational time, thus making it fit to be used in real time where the modulations indices (MI) may vary frequently and for every new MI we need to calculate a new set of switching instants.

References

[1] A. Darvishi, A.Alimardani and S.H. Hosseinian, "Fuzzy Multi-Objective Technique Integrated with Differential Evolution Method to Optimise Power Factor and Total Harmonic Distortion," *IET Generation Transmission and Distribution*, vol. 5, iss. 9, pp. 921–929, 2011.

[2] Mahalekshmi, T., "Current Harmonic Compensation and Power Factor Improvement by Hybrid Shunt Active Power Filter", *Int. J. Comput. Appl*., 4, (3), pp. 9–13, 2010.

[3] B.Srava and B.Seshur, "Elimination Of Harmonic Contents in a Cascaded Multilevel Inverter using Adaptive Hybrid Technique", *International Journal of Current Engineering and Technology*, vol.3, no.5, pp.1606-1610, December 2013.

[4] Ibrahim Gunes, Bulent Ustuntepe and Ahmet M. Hava, " Modern Transformerless Uninterruptable Power Supply (UPS) Systems", *International Conference on Electrical and Electronics Engineering*, ELECO 2009, pp. I-316 - I-320 , Nov. 2009.

[5] Bangyin Liu, Shanxu Duan, Yong Kang, Jian Chen, "Genetic Algorithm Optimized Fuzzy Repetitive Controller for Low Cost UPS Inverter Application", *International Conference on Electric Machines and Drives*, San Antonio, TX, pp. 840 – 845, May 2005.

[6] Jain, P.K., Espinoza, J.R., Jin, H., "Performance of a Single-Stage UPS System for Single-Phase Trapezoidal-Shaped AC-Voltage Supplies", *IEEE Trans. Power Electron*, 13, (5), pp. 912–923., 1998.

[7] Tsung Tsai, M., Hung Liu, C., "Design and Implementation of a Cost Effective Quasi Line-Interactive UPS with Novel Topology", *IEEE Trans. Power Electron*., 18, (4, pp. 1002–1011), 2003.

[8] Nupur Mittal, Bindeshwar Singh, S.P Singh, Rahul Dixit, and Dasharath Kumar, " Multilevel Inverters: A Literature Survey on Topologies and Control Strategies", *IEEE 2nd International Conference on Power, Control and Embedded Systems*,2012.

[9] José Rodríguez, Jih-Sheng Lai, and Fang Zheng Peng,, "Multilevel Inverters: A Survey of Topologies,Controls, and Applications", *IEEE Trans. on Industrial Electronics*, vol. 49, no. 4, pp 724-738, Aug 2002.

[10] Wells, J.R., Geng, X., Chapman, P.L., Krein, P.T., Nee, B.M., "Modulation-Based Harmonic Elimination", *IEEE Trans. Power Electron*., 22, (1), pp. 336–340, 2007.

[11] Ghennam, T., Darwish, M., "A Hybrid Parallel Active Filter/Off-Line UPS Unit for Computer Loads", *Electr. Power Qual. Utilisation J*., 14,(2), pp. 41–48, 2008.

[12] Saied, B.M., Alias, Q.M., AL-soufy, A.S., "Intelligent Systems Based Selective Harmonic Elimination (SHE) for Single Phase Voltage Source Inverter", *Al-Rafidain Eng. J*, 16, (3), pp. 71– 80, 2008.

[13] Dahidah, M.S.A., Agelidis, V.G., "Selective Harmonic Elimination PWM Control for Cascaded Multilevel Voltage Source Converters: a Generalized Formula", *IEEE Trans. Power Electron*.,23, (4), pp. 1620–1630, 2008.

[14] Du, Z., Tolbert, L.M., Chiasson, J.N., Ozpineci, B., "Reduced Switching-Frequency Active Harmonic Elimination for Multilevel Converters", *IEEE Trans. Ind. Electron.*, 55, (4), pp. 1761–1770, 2008.

[15] Jagdish Kumar, Biswarup Das, and Pramod Agarwal, "Selective Harmonic Elimination Technique for a Multilevel Inverter ", *Fifteenth National Power Systems Conference (NPSC)*, IIT Bombay, pp 608-613 , December 2008

[16] Faiz, J., Shahgholian, G., "Modeling and Simulation of a Three-Phase Inverter with Rectifier-Type Nonlinear Loads", *Armenian J. Phys.*, 2, (4), pp. 307–316, 2009.

[17] Faiz, J., Shahgholian, G., Mahdavian, M., "Analysis and Simulation of a three-Phase UPS Inverter with Output Multiple-Filter", *Armenian J. Phys.*, 2, pp. 317–325, 2002.

[18] Bhoopal, N., Madhav, G.V., "Neural and Neuro-Fuzzy Controllers for UPS Inverter Applications", *Int. J. Recent Trends Eng.*, 2, (8), pp. 45–49, 2009.

[19] Du, Z., Tolbert, L.M., Ozpineci, B., Chiasson, J.N., "Fundamental Frequency Switching Strategies of a Seven-Level Hybrid Cascaded H-Bridge Multilevel Inverter", *IEEE Trans. Power Electron*., 24, (1), pp. 25–33, 2009.

[20] Salam, Z., "An on-Line Harmonic Elimination Pulse Width Modulation Scheme for Voltage Source Inverter", *J. Power Electron*., 10, (1), pp. 43–50, 2010,

[21] Nayeripour, Khorsand, Roosta, Niknam,,"A New Approach Based on Fuzzy Controller for Volt/Var Control in Distribution System", *Aus. J. Bas c Appl. Sci.*, 4, (3), pp. 468–480, 2010.

[22] Al-Othman, A.K., Al-Mekhaizim, H.A., "Harmonics elimination in multilevel inverter using linear fuzzy regression', *World Acad. Sci. Eng. Technol*., 62, pp. 194–197, 2010.

[23] Zainal Salam and N.Bahari,, "Selective Harmonics Elimination PWM (SHEPWM) Using Differential Evolution Approach", IEEE, 2010.

[24] Reza Salehithe, R., Farokhnia, N., Abedi, M., Fathi, S.H.: "Elimination of Low Order Harmonics in Multilevel Inverters Using Genetic Algorithm",*J. Power Electron*., 11, (2), pp. 132–139, 2011.

[25] Azab, M.,"Harmonic Elimination in Three-Phase Voltage Source Inverters by Particle Swarm Optimization", *J. Electr. Eng. Technol*., 6, (3), pp. 334–341, 2011.

[26] Merry Geisa, J., Rajaram, M.: "Selective Elimination Of Harmonic Contents In An UPS Using Novel Adaptive Hybrid Technique", *Eur. J. Sci. Res*., 64, (1), pp. 103–114, 2011.

[27] Antony Albert, A.V., Rajasekaran, V., Selvaperumal, S., "Harmonic Elimination of H-Bridge Seven Level Inverter", *Eur. J. Sci. Res.*, 65, (4), pp. 594–600, 2011.

[28] Pandi Perumal, M., Nanjudapan, D.,"Performance Enhancement Of Embedded System Based Multilevel Inverter Using Genetic Algorithm", J. Electr. Eng., 62, (4), pp. 190–198, 2011.

[29] Venkatramanan, C.B., Jayakumar, K.S., Yuvarani, B.,"SHE-PWM Control for Cascaded Voltage Source Multilevel Inverter Based on GA Optimization", *Eur. J. Sci. Res.,* 69, (3), pp. 449–460, 2012.

[30] Mitali Shrivastava, Varsha Singh and Swapnajit Pattnaik,"Artificial Neural Network Based Harmonic Optimization of Multilevel Inverter to Reduce THD", *Proc. of the Intl. Conf. on Advances in Computer, Electronics and Electrical Engineering*, pp.229-233, 2012.

[31] Ayoub Kavousi, Behrooz Vahidi, Reza Salehi, Mohammad Kazem Bakhshizadeh, Naeem Farokhnia and S. Hamid Fathi, "Application of the Bee Algorithm for Selective Harmonic Elimination Strategy in Multilevel Inverters", IEEE Trans on Power Electronics, vol. 27, no. 4, pp.1689-1696, April 2012.

[32] Suman Debnath and Rup Narayan Ray, "Harmonic Elimination in Multilevel Inverter using GA and PSO:A Comparison", IEEE Students Conference on Electrical, Electronics and Computer Science, 2012.

[33] Merry Geisa and M. Rajaram,"Selective Elimination of Harmonic Contents in an Uninterruptible Power Supply: an Enhanced Adaptive Hybrid Technique", *IET Power Electronics*, vol. 5, Iss. 8, pp. 1527–1534, 2012.

[34] Prashanth L Gopal, F.T Josh, "Elimination of Lower Order Harmonics in Multilevel Inverters Using Genetic Algorithm", *International Journal of Engineering and Advanced Technology*, vol-2, issue-3, pp.215-220, February 2013.

[35] Rupali Mohanty, Sthitaprajna Rath and Surya Prasad Mishra, "A Comparison Study of Harmonic Elimination in Cascade Multilevel Inverter Using Particle Swarm Optimization And Genetic Algorithm", *IOSR Journal of Electrical and Electronics Engineering*, vol 5, iss.1, PP. 43-49, Mar. - Apr. 2013

[36] Ali Ajami, Mohammad Reza Jannati Oskuee, and Ata Ollah Mokhberdoran, "Implementation of Novel Technique for Selective Harmonic Elimination in Multilevel Inverters Based on ICA", *Advances in PowerElectronics, Hindawi Publishing Corporation*, pp.1-10, May 2013..

[37] B.Srava and B.Seshur, "Elimination of Harmonic Contents in a Cascaded Multilevel Inverter using Adaptive Hybrid Technique", International Journal of Current Engineering and Technology, vol.3, no.5, pp.1606-1610, Dec 2013.